WHAT IS CLAIMED IS:

1. A method of forming an integrated circuit, comprising:

forming a via opening through first and second dielectric layers located over a conductive layer, the via extending through an interface of the first and second dielectric layers to form a passing metal feature of an interconnect structure; and

forming a trench in the second dielectric layer, wherein the trench opening is not formed at the interface of the first and second dielectric layers.

2. The method as recited in Claim 1 wherein the via opening is a first via opening and the method further includes forming a second via opening through the first and second dielectric layers.

3. The method as recited in Claim 2 wherein the trench is a first trench located approximate the first via opening and the method further includes forming a second trench over the second via opening.

4. The method recited in Claim 3 further including etching through an etch stop and to the first dielectric layer, the etch

stop located at the interface of the first and second dielectric layer.

5. The method as recited in Claim 1 wherein forming a trench includes depositing a photoresist over the second dielectric layer and in the via opening and forming an opening in the photoresist through which the trench is formed.

6. The method as recited in Claim 1 further including forming, prior to forming a via opening, the conductive layer, forming a first etch stop layer comprising silicon nitride over the conductive layer, forming a first dielectric layer over the first etch stop layer, forming a second etch stop layer comprising silicon nitride over the first dielectric layer, and forming a second dielectric layer over the second etch stop layer.

7. The method as recited in Claim 1 including forming a conductive copper layer and forming a first etch stop layer over the conductive copper layer and forming a second etch stop layer over the first dielectric layer.

8. The method as recited in Claim 1 further including depositing a conductive material in the via opening and the trench.

9. The method as recited in Claim 8 wherein depositing a conductive material includes depositing copper in the via opening and the trench.

10. The method as recited in Claim 1 wherein forming the via opening through the first and second dielectric layers includes forming the via with a single photolithographic mask.

11. A method of forming an integrated circuit, comprising:

forming a first dielectric layer over a first metal feature;

forming a second dielectric layer over the first dielectric layer; and

forming from a single photolithographic mask a via opening that extends through the first and second dielectric layers such that the via opening is void of a landing pad at an interface of the first and second dielectric layers, the via extending between the first metal feature and a second metal feature located over the second dielectric layer.

12. The method as recited in Claim 11 wherein the via opening is a first via opening and the method further includes forming a second via opening through the first and second dielectric layers and to a first etch stop layer located over the first metal feature.

13. The method as recited in Claim 12 further including forming a first trench approximate the first via opening and a second trench over the second via opening and to a second etch stop layer located over the first dielectric layer.

14. The method recited in Claim 11 further including forming a landing pad in a surface of the second dielectric layer, forming a third dielectric layer over the second dielectric layer and forming a via opening through the third dielectric layer and to the landing pad.

15. The method as recited in Claim 11 wherein forming a trench includes depositing a photoresist over the second dielectric layer and in the via opening and forming an opening in the photoresist through which the trench opening is formed.

16. The method as recited in Claim 11 further including forming, prior to forming a via opening, the first metal feature, forming a first etch stop layer comprising silicon nitride over the first metal feature, forming a first dielectric layer over the first etch stop layer, forming a second etch stop layer comprising silicon nitride over the first dielectric layer, and forming a second dielectric layer over the second etch stop layer.

17. The method as recited in Claim 11 wherein the first metal feature includes copper and the first and second dielectric layers includes silicon dioxide.

18. The method as recited in Claim 11 further including depositing a conductive material in the via opening.

19. The method as recited in Claim 18 wherein depositing a conductive material includes depositing copper in the via opening.

20. The method as recited in Claim 11 further including forming transistors selected from the group consisting of:

a complementary metal oxide semiconductor device,

a bipolar complementary metal oxide semiconductor device, and

a bipolar semiconductor device.

21. A semiconductor device, comprising:

a first metal feature located over a semiconductor surface and having a first dielectric layer located thereover and a second dielectric layer located over the first dielectric layer, the second dielectric layer having a second metal feature located in a surface thereof; and

a via located through the first and second dielectric layers, the via extending between and connecting the first metal feature and the second metal feature, the via being void of a landing pad between the first and second dielectric layers.

22. The semiconductor device as recited in Claim 21 wherein the via is a first via and the semiconductor device further includes a second via located through the first and second dielectric layers and wherein a trench structure is located over and connects with the second via.

23. The semiconductor device as recited in Claim 21 further including a trench structure located adjacent the via.

24. The semiconductor device as recited in Claim 21 wherein the via is a passing metal via with no passing metal feature.

25. The semiconductor device as recited in Claim 21 further including transistors wherein the first metal feature is located over the transistors and interconnects the transistors to form an operative integrated circuit.

26. The semiconductor device as recited in Claim 21 further including a damascene structure located adjacent the via.

27. The semiconductor device as recited in Claim 21 further including a third dielectric layer located over the second dielectric layer and a landing pad located between the second dielectric layer and the third dielectric layer.

28. The semiconductor device as recited in Claim 27 further including a via that extends through the third dielectric layer and contacts the landing pad.